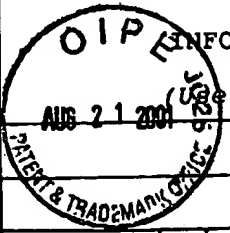


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 INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANT Eliyahou Harari et al.									
				FILED May 30, 2001		GROUP 2824							
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AT	A1	4	0	9	0	2	5	8	1978	Cricchi			
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	A3	4	2	7	9	0	2	4	1981	Schrenk			
AT	A4	4	3	5	7	6	8	5	1982	Daniele et al.			
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AT	B1	2	0	6	1	6	5	1	1981	United Kingdom			
AT	B2	5	9	3	1	1	5	8	1984	Japanese Pat. Publica.			YES
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	C2	Torelli et al., "Single Chip, 16-Station TV Digital Tuning System," <i>SGS-ATES Technical Note</i> 170, pp. 1-19 (1984)											
	C3	Torelli et al., "PLL2K-PLL Frequency Synthesizer For 30 Programs," <i>SGS-ATES Componenti Electronici SpA</i> , Technical Note 152, pp. 1-16 (1982)											
	C4	Scrocchi et al., "EPM32-Electronic Program Memory System For TV (32 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , Technical Note 153, pp. 1-19 (1982)											
	C5	"EPM 16-Electronic Program Memory (16 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M193A-M193C-M193D, 15 pps, (November, 1981)											
	C6	"EPM-32 Electronic Program Memory (32 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M293, 16 pps. (October, 1982)											
AT	C7	"Single Chip Non-Volatile Station Memory, PCM Remote Control Receiver and Display Driver," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M490-M491, 24 pps. (May, 1983)											
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	A6 4 7 1 8 0 4 1	1988	Baglee et al.			
	A7 4 7 6 3 3 0 5	1988	Kuo			
	A8 4 8 0 5 1 5 1	1989	Terada et al.			
	A9 4 8 1 1 2 9 4	1989	Kobayashi et al.			
	A10 5 0 5 3 9 9 0	1991	Kreifels et al.			
AT	A11 5 0 9 5 3 4 4	1992	Harari			

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B3 6 2 2 5 7 6 9 9	1987	Japan			Abstr

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AT	C8	"PLL TV Microcomputer Interface," <u>SGS-ATES Componenti Electronici SpA</u> , MOS Integrated Circuits/M290, 15 pps. (June, 1982)
	C9	Gee et al., "An Enhanced 16K E ² PROM," <u>IEEE Journal of Solid State Circuits</u> , Vol. SC-17, No. 5 (Oct. 1982)
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AT	C12	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver In A Single Chip," <u>IEEE Digest of Technical Papers</u> , Cat. No. 83CH1872-1, 2pp. (June, 1983)

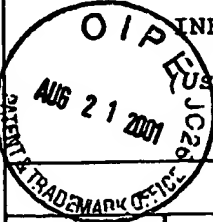
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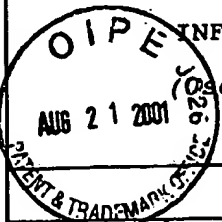
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*EXAMINER INITIAL		DOCUMENT NUMBER				DATE	NAME	CLASS	SUB CLASS	FILING DATE	
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AT	C13	Torelli et al., "Non-Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-29, No. 3, pp. 103-13 (Aug. 1983)									
	C14	Excerpts from a 1983 Data Book published by SGS-ATES Group, 45 pp. (Nov. 1983)									
	C15	Berenga et al., "E ² -PROM TV Synthesizer," <u>IEEE Digest of Technical Papers</u> , Cat. No. 78CH1298-9SSC, 4 pp. (Feb. 1978)									
	C16	Klingman, "Microprocessor Systems Design," <u>Prentice-Hall, Inc.</u> , pp. 30-31 (1977)									
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	C18	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987)									
AT	C19	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)									
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AT	C20	Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," <u>IBM Technical Disclosure Bulletin</u> , Vol. 24, No. 7A, pps. 3311-3314 (December 1981)					
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	A19 4 7 7 9 2 7 2	10/18/88	Kohda et al.			
	A20 4 7 5 2 9 2 9	6/21/88	Kantz et al.			
	A21 4 8 7 0 6 1 8	9/26/89	Iwashita			
	A22 4 6 1 2 6 2 9	9/16/86	Harari			
	A23 4 7 9 9 1 9 5	1/17/89	Iwahashi et al.			
	A24 4 7 3 3 3 9 4	3/22/88	Giebel			
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	A26 4 4 6 0 9 8 2	7/17/84	Gee et al.			
	A27 5 1 6 3 0 2 1	11/10/92	Mehrotra et al.			
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	A29 5 6 0 2 9 8 7	2/92	Harari et al.			
	A30 5 2 9 7 1 4 8	3/94	Harari et al.			
AT	A31 5 0 0 3 5 1 0	3/91	Hamisaki			

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*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
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	C22	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, <u>IEEE</u> , (1988)
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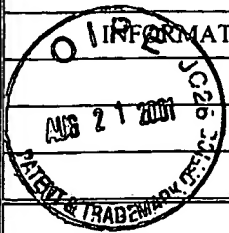
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					11587 M-10187-43C US		09/867,836	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)					Applicant(s)			
					Eliyahou Harari et al.			
					Filing Date		Group	
					May 30, 2001		2824	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
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	AJ							
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
AT	AL	60-15896	Jan. 26, 1985	Japan	G11C	17/00	Yes	
	AM	62-188100	Aug. 17, 1987	Japan	G11C	17/00	Yes	
	AN	62-52798	Mar. 7, 1987	Japan	G11C	17/00	Abstract	
	AO	62-76098	Apr. 8, 1987	Japan	G11C	17/00	Abstract	
	AP	62-80899	Apr. 14, 1987	Japan	G11C	17/00	Abstract	
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	AS							
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Use several sheets if necessary)					Eliyahou Harari et al.			
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							Translation	
	Document	Date	Country	Class	Subclass	Yes	No	
	AL							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
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	AS							
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				Applicants		Conf. No.	
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(Form PTO-1449)				Filing Date		Art Group	
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	2	4,677,590	6/30/87	Arakawa			
	3	4,691,298	9/1/87	Fukuda et al.			
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AT	18	DE 3831538 A1	30/3/89	Germany	G11C	17/06	Abstract	X
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AT	21	SEEQ Data Book 1988/89, SEEQ Technology, Inc., pp. 3-1-3-7.
AT	22	USPTO, Office Action mailed in Application No. 09/635,597 on August 22, 2005, 12 pages.

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	24	Kynett, Virgil Niles et al., "A 90-ns One-Million Erase/Program Cycle 1-Mbit Flash Memory," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1259-1264.	
	25	IBM Technical Disclosure Bulletin, "EPROM Programming Device," Vol. 29, No. 9, February 1987, pp. 4145-4146.	
	26	Tanaka, Tomoharu et al., "A 4-Mbit NAND-EEPROM with Tight Programmed Vt Distribution," 1990 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 105-106.	
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